AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double-bracketed text indicating deletions.

1. (Original) A sense amplifying circuit, comprising:

a selecting unit for selecting one pair from a first pair of a first signal and a first inverted signal and a second pair of a second signal and a second inverted signal, the selecting unit selecting the one pair in response to a selection signal and an inverted selection signal;

a sensing unit for sensing voltage levels of one pair of signals selected from the first pair and the second pair;

a latching unit for precharging first and second nodes in response to a clock signal and for controls voltage levels of the first and second nodes in response to a sensing result of the sensing unit;

an output unit for inverts the voltage levels of the first and second nodes to generate first and second output signals; and

a switching unit for controlling the operation of the selecting unit in response to the clock signal.

2. (Original) The sense amplifying circuit of claim 1, wherein the latching unit comprises:

a first precharge transistor including a first end connected to a power voltage, a second end connected to the first node, and a gate connected to the clock signal;

a second precharge transistor including a first end connected to the power voltage, a second end connected to the second node, and a gate connected to the clock signal;

a first latch transistor including a first end connected to the power voltage, a second end connected to the first node, and a gate connected to the second node;

a second latch transistor including a first end connected to the power voltage, a second end connected to the second node, and a gate connected to the first node;

third and fourth transistors including first ends connected to the first node and gates connected to the second node; and

fifth and sixth transistors including first ends connected to the second node and gates connected to the first node.

3. (Original) The sense amplifying circuit of claim 2, wherein the latching unit further comprises:

a first current pass transistor including a first end connected to the first node, a second end connected to the switching unit, and a gate connected to the second node; and

a second current pass transistor including a first end connected to the second node, a second end connected to the switching unit, and a gate connected to the first node.

4. (Original) The sense amplifying circuit of claim 2, wherein the sensing unit comprises:

a first sense transistor including a first end connected to a second end of the third latch transistor and a gate connected to the first signal;

a first inverted sense transistor including a first end connected to a second end of the sixth latch transistor and a gate connected to the first inverted signal;

a second sense transistor including a first end connected to a second end of the fourth latch transistor and a gate connected to the second signal; and

a second inverted sense transistor including a first end connected to a second end of the fifth latch transistor and a gate connected to the first inverted signal.

5. (Original) The sense amplifying circuit of claim 4, wherein the selecting unit comprises:

a first select transistor including a first end connected to a second end of the first sense transistor and a second end of the first inverted sense transistor, a gate connected to the selection signal, and a second end connected to a third node; and

a second select transistor including a first end connected to the second end of the second sense transistor and the second end of the second inverted sense transistor, a gate connected to the inverted selection signal, and a second end connected to the third node.

6. (Original) The sense amplifying circuit of claim 4, wherein the selecting unit comprises:

a first select transistor including a first end connected to a second end of the first sense transistor, a gate connected to the selection signal, and a second end connected to the third node;

a first inverted select transistor including a first end connected to a second end of the first inverted sense transistor, a gate connected to the selection signal, and a second end connected to the third node;

a second select transistor including a first end connected to a second end of the second sense transistor, a gate connected to the inverted selection signal, and a second end connected to the third node; and

a second inverted select transistor including a first end connected to a second end of the second inverted sense transistor, a gate connected to the inverted selection signal, and a second end connected to the third node.

7. (Original) The sense amplifying circuit of claim 5, wherein the switching unit is a switch transistor includes a first end connected to the third node, a gate connected to the clock signal, and a second end connected to a ground voltage.

8. (Original) The sense amplifying circuit of claim 7, wherein the first and second precharge transistors and the first and second latch transistors are PMOS transistors, and the third through sixth latch transistors, the first and second sense transistors, the first and second inverted sense transistors, the first and second select transistors, the first and second inverted select transistors, and the switch transistor are NMOS transistors.

9. (Original) A sense amplifying circuit comprising:

a selecting unit for selecting one pair from a first pair of a first signal and a first inverted signal and a second pair of a second signal and a second inverted signal, in response to a first level of a clock signal, a selection signal, and an inverted selection signal;

a sensing unit for sensing voltage levels of one pair of signals selected from the first and second pairs;

a latching unit for precharging first and second nodes in response to a second level of the clock signal and controls voltage levels of the first and second nodes in response to a sensing result of the sensing unit; and

an output unit for inverting the voltage levels of the first and second nodes to generate first and second output signals.

10. (Original) The sense amplifying circuit of claim 9, wherein the latching unit comprises:

a first precharge transistor including a first end connected to a power voltage, a second end connected to the first node, and a gate connected to the clock signal;

a second precharge transistor including a first end connected to the power voltage, a second end connected to the second node, and a gate connected to the clock signal;

a first latch transistor including a first end connected to the power voltage, a second end connected to the first node, and a gate connected to the second node;

a second latch transistor including a first end connected to the power voltage, a second end connected to the second node, and a gate connected to the first node;

third and fourth transistors including first ends connected to the first node and gates connected to the second node; and

fifth and sixth transistors including first ends connected to the second node and gates connected to the first node.

11. (Original) The sense amplifying circuit of claim 10, wherein the sensing unit comprises:

a first sense transistor including a first end connected to a second end of the third latch transistor and a gate connected to the first signal;

a first inverted sense transistor including a first end connected to a second end of the sixth latch transistor and a gate connected to the first inverted signal;

a second sense transistor including a first end connected to a second end of the fourth latch transistor and a gate connected to the second signal; and

a second inverted sense transistor including a first end connected to a second end of the fifth latch transistor and a gate connected to the first inverted signal.

12. (Original) The sense amplifying circuit of claim 11, wherein the selecting unit comprises:

a first switch transistor including a first end connected to a second end of the first sense transistor and a second end of the first inverted sense transistor, and a gate connected to the clock signal;

a second switch transistor including a first end connected to a second end of the second sense transistor and a second end of the second inverted sense transistor, and a gate connected to the clock signal;

a first select transistor including a first end connected to a second end of the first switch transistor, a gate connected to the selection signal, and a second end connected to a ground voltage; and

a second select transistor including a first end connected to a second end of the second switch transistor, a gate connected to the inverted selection signal, a second end connected to the ground voltage.

13. (Original) The sense amplifying circuit of claim 11, wherein the selecting unit comprises:

a first switch transistor including a first end connected to a second end of the first sense transistor and a gate connected to the clock signal;

a first inverted switch transistor including a first end connected to a second end of the first inverted sense transistor and a gate connected to the clock signal;

a second switch transistor including a first end connected to a second end of the second sense transistor and a gate connected to the clock signal;

a second inverted switch transistor that comprises a first end connected to a second end of the second inverted sense transistor and a gate connected to the clock signal;

a first select transistor including a first end connected to second ends of the first switch transistor and the first inverted switch transistor, a gate connected to the selection signal, and a second end connected to the ground voltage; and

a second select transistor including a first end connected to second ends of the second switch transistor and the second inverted switch transistor, a gate connected to the inverted selection signal, and a second end connected to the ground voltage.

14. (Original) The sense amplifying circuit of claim 11, wherein the selecting unit comprises:

a first switch transistor including a first end connected to a second end of the first sense transistor and a gate connected to the clock signal;

a first inverted switch transistor including a first end connected to a second end of the first inverted sense transistor and a gate connected to the clock signal;

a second switch transistor including a first end connected to a second end of the second sense transistor and a gate connected to the clock signal;

a second inverted switch transistor including a first end connected to a second end of the second inverted sense transistor and a gate connected to the clock signal;

a first select transistor including a first end connected to a second end of the first switch transistor, a gate connected to the selection signal, and a second end connected to the ground voltage;

a first inverted select transistor including a first end connected to a second end of the first inverted switch transistor, a gate connected to the selection signal, and a second end connected to the ground voltage;

a second select transistor including a first end connected to a second end of the second switch transistor, a gate connected to the inverted selection signal, and a second end connected to the ground voltage; and

a second inverted select transistor including a first end connected to a second end of the second inverted switch transistor, a gate connected to the inverted selection signal, a second end connected to the ground voltage.

15. (Original) The sense amplifying circuit of claim 14, wherein the first and second precharge transistors and the first and second latch transistors are PMOS transistors, and the third through sixth latch transistors, the first and second sense transistors, the first and second inverted sense transistors, the first and second select transistors, the first and second inverted select transistors, and the first through fourth switch transistors are NMOS transistors.

16. (Original) A bit comparator comprising:

a random access memory cell for receiving and storing data and inverted data having an opposite level to the data from a pair of data lines to generate a selection signal and an inverted selection signal in response to a control signal;

a selecting unit for selecting one pair from a first pair of first signal and first inverted signal and a second pair of second signal and second inverted signal in response to a first level of a clock signal, the selection signal, and the inverted selection signal;

a sensing unit for sensing voltage levels of one pair of signals selected from the first and second pairs;

a latching unit for precharging first and second nodes in response to a second level of the clock signal and controls voltage levels of the first and second nodes in response to a sensing result of the sensing unit; and

an output unit for inverting the voltage levels of the first and second nodes to generate first and second output signals and determines in response to a level of the second output signal whether the data and the inverted data coincide with the first signal and the first inverted signal.

17. (Original) The bit comparator of claim 16, wherein the random access memory cell comprises:

a data maintainer including first and second inverters, an output of the first inverter being connected to an input of the second inverter and an input of the first inverter being connected to an output of the second inverter;

a first control transistor for transmitting the data to an input node of the first inverter via one of the pair of data lines in response to the control signal; and

a second control transistor for transmitting the inverted data to an input node of the second inverter via the other one of the pair of data lines in response to the control signal,

wherein the pair of data lines is a pair of bit lines.

18. (Original) The bit comparator of claim 16, wherein the data is equal to the selection signal, the inverted data is equal to the inverted selection signal, the first signal is equal to the second inverted signal, the second signal is equal to the first inverted signal, and the first signal and the first inverted signal have opposite levels and are address data input to the bit comparator.

19. (Original) The bit comparator of claim 16, wherein in the sensing unit, when the clock signal and the selection signal are at a first level, a first sense transistor includes a gate to which the first signal is applied and a first inverted sense transistor comprising a gate to which the first inverted signal is applied are turned on and a source of the first sense transistor is connected to a source of the first inverted sense transistor, and when the clock signal and the inverted selection signal are at the first level, a second sense transistor includes a gate to which the second signal is applied and a second inverted sense transistor comprising a gate to which the second inverted signal is applied are turned on and a source of the second sense transistor is connected to a source of the second inverted sense transistor.

20. (Original) The bit comparator of claim 19, wherein the selecting unit comprises:

a first switch transistor including a first end connected to sources of the first sense transistor and the first inverted sense transistor and a gate connected to the clock signal;

a second switch transistor including a first end connected to sources of the second sense transistor and the second inverted sense transistor and a gate connected to the clock signal;

a first select transistor including a first end connected to a second end of the first switch transistor, a gate connected to the selection signal, and a second end connected to a ground voltage; and

a second select transistor including a first end connected to a second end of the second switch transistor, a gate connected to the inverted selection signal, and a second end connected to the ground voltage.

21. (Original) The bit comparator of claim 19, wherein the selecting unit comprises:

a first select transistor including a first end connected to sources of the first sense transistor and the first inverted sense transistor and a gate connected to the selection signal;

a second select transistor including a first end connected to sources of the second sense transistor and the second inverted sense transistor and a gate connected to the inverted selection signal;

a first switch transistor including a first end connected to a second end of the first select transistor, a gate connected to the clock signal, and a second end connected to a ground voltage; and

a second switch transistor including a first end connected to a second end of the second select transistor, a gate connected to the clock signal, and a second end connected to the ground voltage.

22. (Original) The sense amplifying circuit of claim 6, wherein the switching unit is a switch transistor includes a first end connected to the third node, a gate connected to the clock signal, and a second end connected to a ground voltage.

23. (Original) An apparatus, comprising:

a selecting unit for selecting a signal pair from at least two pairs of signals, the selecting unit selecting the signal pair based upon at least one selection signal; and

amplifying circuitry for amplifying only the signal pair selected from the at least two pairs of signals.

24. (Original) The apparatus according to claim 23, wherein the selecting unit selects the signal pair based upon a selection signal and an inverted selection signal.

25. (Original) The apparatus according to claim 24, wherein the inverted selection signal is obtained by inverting the selection signal.

26. (Original) A method, comprising:

selecting a signal pair from at least two pairs of signals based upon at least one selection signal; and

amplifying only the signal pair selected from the at least two pairs of signals.

27. (New) The apparatus according to claim 23, further comprising:

a sensing unit for sensing voltage levels of one pair of signals selected from the at least two pairs;

a latching unit for precharging first and second nodes in response to a clock signal and for controlling voltage levels of the first and second nodes in response to a sensing result of the sensing unit;

an output unit for inverts the voltage levels of the first and second nodes to generate first and second output signals; and

a switching unit for controlling the operation of the selecting unit in response to the clock signal.

28. (New) The method according to claim 26,

sensing voltage levels of the selected signal pair;

precharging first and second nodes in response to a clock signal;

controlling the voltage levels of the first and second nodes in response to the sensing;

inverting the voltage levels of the first and second nodes to generator first and second output signals; and

controlling the operation of the selecting unit in response to the clock signal